Listing of Claims

1. (Canceled).

2. (Currently Amended) A method for synchronizing a data interchange in a semiconductor substrate integrated electronic circuit comprising a transmitter block and a receiver block connected through a communication network, comprising:

generating a data signal having a transmission period on a first line, the data signal ~~that is~~ sent at a first instant from said transmitter block to be received by the receiver block;

generating on a second line a congestion signal sent from the receiver block to the transmitter block when a congestion event of the receiver block occurs in order to interrupt the transmission of said data signal; and

generating on a third line a synchro signal sent at a second instant from said transmitter block, this synchro signal indicating to the receiver block that the data signal on the first line comprises a new datum,

wherein the congestion signal interrupts also the transmission of said synchro signal when a congestion event of the receiver block occurs, and

wherein the second instant for sending ~~generating~~ said synchro signal for communication over the third line is delayed with respect to the first instant for sending ~~generating~~ the data signal for communication over the first line.

3. (Previously Presented) The method for synchronizing the data interchange according to claim 2, wherein said synchro signal is delayed by a half transmission period with respect to the data signal.

4. (Currently Amended) A method for synchronizing a data interchange in a semiconductor substrate integrated electronic circuit comprising a transmitter block and a receiver block connected through a communication network, comprising:

generating a data signal having a transmission period on a first line that from said transmitter block must be received by the receiver block;

generating on a second line a congestion signal from the receiver block to the transmitter block when a congestion event of the receiver block occurs in order to interrupt the transmission of said data signal;

generating on a third line a synchro signal starting from said transmitter block, this synchro signal indicating to the receiver block that the data signal comprises a new datum, and in that the congestion signal interrupts also the transmission of said synchro signal when a congestion event of the receiver block occurs; and

reading, by the receiver block, of the data signal with a different sampling period than the transmission period of the transmitter block, wherein sampling by the receiver block for reading in accordance with the different sampling period occurs simultaneously with reception by the receiver block of the synchro signal.

5. (Currently Amended) A method for synchronizing a data interchange in a semiconductor substrate integrated electronic circuit comprising a transmitter block and a receiver block connected through a communication network, comprising:

generating a data signal having a transmission period on a first line that from said transmitter block must be received by the receiver block;

generating on a second line a congestion signal from the receiver block to the transmitter block when a congestion event of the receiver block occurs in order to interrupt the transmission of said data signal;

generating on a third line a synchro signal starting from said transmitter block, this synchro signal indicating to the receiver block that the data signal comprises a new datum, and in that the congestion signal interrupts also the transmission of said synchro signal when a congestion event of the receiver block occurs; and

reading, by the receiver block, of the data signal with a different sampling period than the transmission period of the transmitter block;

wherein the different sampling period is a shorter sampling period than the transmission period of the transmitter block and sampling in accordance with that shorter sampling period occurs simultaneously with reception by the receiver block of the synchro signal.

6. (Previously Presented) A method for synchronizing a data interchange in a semiconductor substrate integrated electronic circuit comprising a transmitter block and a receiver block connected through a communication network, comprising:

generating a data signal having a transmission period on a first line that from said transmitter block must be received by the receiver block;

generating on a second line a congestion signal from the receiver block to the transmitter block when a congestion event of the receiver block occurs in order to interrupt the transmission of said data signal; and

generating on a third line a synchro signal starting from said transmitter block, this synchro signal indicating to the receiver block that the data signal comprises a new datum, and in that the congestion signal interrupts also the transmission of said synchro signal when a congestion event of the receiver block occurs,

wherein said first, second and third lines are split in corresponding stages, each stage being separated through a corresponding repeater, the repeaters of the first and third lines being of the tristate type and being driven by the repeater of the second line when a congestion event occurs at the receiver block so that the data signal and the synchro signal are stored in the stages of the first and third lines; and

wherein said stages have an elementary delay which must be shorter than half the transmission period.

Claims 7-8. (Canceled).

9. (Previously Presented) An integrated electronic circuit being integrated on a semiconductor substrate comprising a transmitter block and a receiver block connected through a communication network, said communication network comprising a first line for a data signal, a second line for a congestion signal, and a third line for a synchro signal, wherein said first, second and third lines are split in corresponding stages, each stage being separated through a corresponding repeater, the repeaters of the first and third lines being of the tristate type whose tristate condition is controlled by an output of the repeater of the second line when a congestion event of the receiver block occurs so that the data signal and the synchro signal are stored in the stages of the first and second lines.

10. (Original) The integrated electronic circuit of claim 9 wherein said signal line comprises a couple of further lines for a couple of unidirectional signals indicating the transmission direction between said transmitter block and said receiver block, a negotiation to define the transmission direction being controlled by a further transmission request signal driven by the receiver block.

Claims 11-13. (Canceled).

14. (Currently Amended) A communication protocol method, comprising:

transmitting from a transmitting entity to a receiving entity ~~along with~~ a data signal and a synchronization signal indicating to the receiving entity that the data signal comprises new datum; and

inhibiting transmission of the synchronization signal by the transmitting entity in response to an indication received from the receiving entity of the existence of a congestion condition at the receiving entity,

wherein the data signal is communicated on a first communication line and the synchronization signal is communicated on a second communication line; and

wherein transmitting from the transmitting entity comprises delaying between a first instant for sending the data signal over the first communications line and a second instant for sending the synchronization signal over the second communication line ~~with respect to sending the data signal over the first communication line~~.

15. (Canceled).

16. (Previously Presented) The protocol method as in claim 14, wherein the indication of the existence of a congestion condition at the receiving entity is received over a third communication line.

17. (Previously Presented) The protocol method as in claim 14 further including inhibiting transmission of the data signal in response to the indication received from the receiving entity of the existence of a congestion condition at the receiving entity.

18. (Canceled).

19. (Previously Presented) A communication system, comprising:

a first communication block;

a second communication block;

a communication network interconnecting the first and second communication blocks, the communication network comprising:

a first communication line for carrying a data signal;

a second communication line for carrying a congestion signal; and

a third communication line for carrying a synchronization signal, wherein the synchronization signal is active whenever the data signal on the first communication line is new datum and inactive whenever the congestion signal on the second communication line is active,

wherein the first, second and third communication lines are each split into corresponding stages, further comprising:

a repeater device separating consecutive ones of the stages; and

wherein the repeaters of the first and third communications lines are of the tristate type whose tristate condition is controlled by an output of the repeater of the second communication line in response to the congestion signal being active so that the data signal and the synchronization signal are stored in stages of the first and second communications lines.

Claims 20-21. (Canceled).

22. (Currently Amended) A communication system, comprising:

a first communication block;

a second communication block;

a communication network interconnecting the first and second communication blocks, the communication network comprising:

a first communication line for carrying a data signal;

a second communication line for carrying a congestion signal; and

a third communication line for carrying a synchronization signal, wherein the synchronization signal is active whenever the data signal on the first communication line is new datum and inactive whenever the congestion signal on the second communication line is active;

wherein the first, second and third communication lines are bi-directional, further including:

a transmit signal line; and

a receive signal line;

wherein the transmit and receive signal lines interconnect the first and second communication blocks, and the first and second communication ~~communications~~ blocks set a logic state of the transmit signal line and receive signal line which specify, for the bi-directional first communication line, which of the first and second communication blocks is a transmitter of the data signal and which of the first and second communication blocks is a receiver of the data signal.

23. (Original) The system of claim 22, further including a request signal line that interconnects the first and second communication blocks, and a control signal thereon used to negotiate which of the first and second communication blocks is to be transmitter/receiver.

24. (Canceled).

25. (Currently Amended) A communication system, comprising:

a first communication block;

a second communication block;

a communication network interconnecting the first and second communication blocks, the communication network comprising:

a first communication line for carrying a data signal;

a second communication line for carrying a congestion signal; and

a third communication line for carrying a synchronization signal, wherein the synchronization signal is active whenever the data signal on the first communication line is new datum and inactive whenever the congestion signal on the second communication line is active;

wherein an instant for ~~the~~ sending of the active synchronization signal transmission over the third communication line is delayed after an instant for ~~with respect to~~ sending of the data signal transmission on the first communication line.